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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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PATTI & BRILL ONE NORTH LASALLE STREET 44TH FLOOR CHICAGO, IL 60602			GUILL, RUSSELL L	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/851,898

Applicant(s)

HALCOMB ET AL.

Examiner

Russell L. Guill

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1 – 20 have been examined. Claims 1 – 20 have been rejected.

Claim Objections

2. Claims 10 and 11 are objected to because of the following informalities: Both claims recite the phrase, “further the step”. For the purpose of claim examination, the phrase is interpreted as, “further comprising the step”. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Independent claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; “The Transmogriifier-2: A 1 Million Gate Rapid-Prototyping System”, June 1998, IEEE Transactions on Very Large Scale Integration Systems), in view of FLEX10K (“FLEX 10K DEVICE FAMILY”, March 2000, web.archive.org/web/20000303160208/www.altera.com/html/products/f10k.html).

- 4.1. The art of Lewis is directed toward a rapid-prototyping system to emulate computer hardware systems (**page 188, Abstract, and section I. Introduction**).

- 4.2. The art of FLEX10K is directed to data regarding the Altera FLEX 10K programmable logic devices.
- 4.3. Lewis appears to teach an apparatus comprising:
- 4.3.1. A programmable logic device (page 188, Abstract; please note that the Altera 10K50 FPGA is a programmable logic device), arranged and constructed to receive a program that programs at least one processor operation into the programmable logic device (page 188, section I. Introduction).
- 4.3.2. A programmable logic device (page 188, Abstract; please note that the Altera 10K50 FPGA is a programmable logic device), arranged and constructed to receive a program that programs a variable clock speed into the programmable logic device (page 188, Abstract; and page 189, left-side column, item 5; and page 195, section F. Clocking).
- 4.3.3. At least one interface device through which the program and the variable clock speed are programmed into the programmable logic device (page 196, left-side column, section G. Status, Power Monitoring, Host Communication, and Boot; and page 196, Figure 8).
- 4.4. Lewis does not specifically teach a programmable logic device, arranged and constructed to receive a program that programs at least one processor operation and a variable clock speed into the programmable logic device.
- 4.5. FLEX10K appears to teach a programmable logic device arranged and constructed to receive a program that programs at least one processor operation (Section: Embedded Array Revolutionizes Programmable Logic) and a variable clock speed (Table 1 FLEX 10K Highlights, column Feature, row Phase-locked loop) into the

programmable logic device (**Section: Embedded Array Revolutionizes Programmable Logic**).

4.6. The art of FLEX10K and the art of Lewis are analogous art because Lewis uses the Altera 10K50 programmable logic device (Lewis, page 188, Abstract), while FLEX10K describes the Altera 10K50 programmable logic device (**FLEX10K: Section: Embedded Array Revolutionizes Programmable Logic**).

4.7. The motivation to use the art of FLEX10K with the art of Lewis would have been obvious because 1) Lewis uses the Altera 10K50 FPGA, and 2) the numerous benefits recited in FLEX10K such as ease-of-use, fast and predictable performance, register-rich architecture, and ability to implement designs that integrate a complete system on a device (**FLEX10K: Section: Embedded Array Revolutionizes Programmable Logic**).

4.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of FLEX10K with the art of Lewis to produce the claimed invention.

5. Dependent claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; "The Transmogripher-2: A 1 Million Gate Rapid-Prototyping System", June 1998, IEEE Transactions on Very Large Scale Integration Systems) and FLEX10K ("FLEX 10K DEVICE FAMILY", March 2000, web.archive.org/web/20000303160208/www.altera.com/html/products/f10k.html), in view of Mitchell (U.S. Patent Number 6,230,119).

5.1. Claim 2 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

- 5.2. The art of Lewis is directed toward a rapid-prototyping system to emulate computer hardware systems (page 188, Abstract, and section I. Introduction).
- 5.3. The art of Mitchell is directed to an emulation system to emulate a processor (column 1, lines 5 - 10).
- 5.4. Lewis does not specifically teach that the programmable logic device has as many pins as a processor for which the at least one processor operation is emulated.
- 5.5. Mitchell appears to teach that the programmable logic device has as many pins as a processor for which the at least one processor operation is emulated (figure 1, elements Microcontroller Emulator, Emulation Pod, and Customer's Target Board; and figure 2, elements Same build in chip used for emulation, and Customer's Target Board).
- 5.5.1. Regarding (figure 1, elements Microcontroller Emulator, Emulation Pod, and Customer's Target Board; and figure 2, elements Same build in chip used for emulation, and Customer's Target Board); it would have been obvious to have a programmable logic device that has as many pins as a processor for which the at least one processor operation is emulated.
- 5.6. The art of Mitchell and the art of Lewis are analogous art because they are both directed to an emulation system.
- 5.7. The motivation to use the art of Mitchell with the art of Lewis would have been obvious because of the benefit recited in Mitchell of utilizing a multiplexed pin in the processor package for communicating internal processor status information to an external system or controller (column 2, lines 41 - 57).

5.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mitchell with the art of Lewis to produce the claimed invention.

6. Dependent claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; "The Transmogripher-2: A 1 Million Gate Rapid-Prototyping System", June 1998, IEEE Transactions on Very Large Scale Integration Systems) and FLEX10K ("FLEX 10K DEVICE FAMILY", March 2000, web.archive.org/web/20000303160208/www.altera.com/html/products/f10k.html), in view of Keenan (U.S. Patent Number 4,903,199).

6.1. Claim 3 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

6.2. The art of Lewis is directed toward a rapid-prototyping system to emulate computer hardware systems (**page 188, Abstract, and section I. Introduction**).

6.3. The art of Keenan is directed to test systems for integrated circuits (**column 1, lines 6 – 12**).

6.4. Lewis and FLEX10 appears to teach a programmable logic device that is arranged and constructed to emulate the at least one processor operation (**Lewis, page 188, Abstract and section I. Introduction**).

6.4.1. Regarding (**Lewis, page 188, Abstract and section I. Introduction**); the Altera 10K50 FPGA is obviously arranged and constructed to emulate at least one processor operation since the TM-2 is a rapid-prototyping emulation system

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- 6.5. Lewis does not specifically teach that the programmable logic device is arranged and constructed to emulate the at least one processor operation repeatedly without interruption.
- 6.6. Keenan appears to teach performing a processor operation repeatedly without interruption (column 1, lines 47 – 57; column 2, lines 25 – 30; and column 6, lines 24 – 30).
- 6.6.1. Regarding (column 1, lines 47 – 57; column 2, lines 25 – 30; and column 6, lines 24 – 30); it would have been obvious to repeatedly test a processor operation without interruption since Keenan teaches performing a test in a loop.
- 6.7. The art of Keenan and the art of Lewis are analogous art because they both contain the problem of testing integrated circuits (Lewis, page 194, section C. Debugging Facilities) and (Keenan, column 1, lines 6 – 12).
- 6.8. The motivation to use the art of Keenan with the art of Lewis would have been obvious because of the benefit recited in Keenan that the method increases the speed of test program execution (column 1, lines 1 – 12).
- 6.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Keenan with the art of Lewis to produce the claimed invention.
7. Independent claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; “The Transmogri-fier-2: A 1 Million Gate Rapid-Prototyping System”, June 1998, IEEE Transactions on Very Large Scale Integration Systems), in view of Keenan (U.S. Patent Number 4,903,199), further in view of Mitchell (U.S. Patent Number 6,230,119).

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- 7.1. The art of Lewis is directed toward a rapid-prototyping system to emulate computer hardware systems (page 188, Abstract, and section I. Introduction).
- 7.2. The art of Keenan is directed to test systems for integrated circuits (column 1, lines 6 – 12).
- 7.3. The art of Mitchell is directed to an emulation system to emulate a processor (column 1, lines 5 – 10).
- 7.4. Lewis appears to teach:
- 7.4.1. Selecting an operation that emulates at least one operation of a processor (page 188, section Introduction).
- 7.4.1.1. Regarding (page 188, section Introduction); it would have been obvious that a system that emulates a processor will have at least one operation of the processor selected.
- 7.4.2. Downloading the operation into a programmable logic device (page 189, right-side column, item 8) Programming Time; page 196, left-side column, section G. Status, Power Monitoring, Host Communicaton, and Boot, first paragraph).
- 7.4.3. Selecting a clock speed at which to operate the programmable logic device (page 195, section F. Clocking; page 196, left-side column, section G. Status, Power Monitoring, Host Communicaton, and Boot, first paragraph).
- 7.4.3.1. Regarding (page 195, section F. Clocking; page 196, left-side column, section G. Status, Power Monitoring, Host Communicaton, and

Boot, first paragraph); it would have been obvious that a clock speed is selected in order to program the clock speed.

- 7.4.4. Programming the programmable logic device to operate at the clock speed (page 195, section F. Clocking; page 196, left-side column, section G. Status, Power Monitoring, Host Communication, and Boot, first paragraph).
- 7.5. Lewis does not specifically teach repeatedly testing the operation in combination with a circuit.
- 7.6. Keenan appears to teach repeatedly testing the operation (column 1, lines 47 – 57; column 2, lines 25 – 30; and column 6, lines 24 – 30).
- 7.7. Mitchell appears to teach testing the processor operation in combination with a circuit (figure 1, elements Microcontroller Emulator, Emulation Pod, and Customer's Target Board; and figure 2, elements Same build in chip used for emulation, and Customer's Target Board).
- 7.8. The art of Keenan and the art of Lewis are analogous art because they both contain the problem of testing integrated circuits (Lewis, page 194, section C. Debugging Facilities) and (Keenan, column 1, lines 6 – 12).
- 7.9. The motivation to use the art of Keenan with the art of Lewis would have been obvious because of the benefit recited in Keenan that the method increases the speed of test program execution (column 1, lines 1 – 12).
- 7.10. The art of Mitchell and the art of Lewis are analogous art because they are both directed to an emulation system.

7.11. The motivation to use the art of Mitchell with the art of Lewis would have been obvious because of the benefit recited in Mitchell of utilizing a multiplexed pin in the processor package for communicating internal processor status information to an external system or controller (**Mitchell, column 2, lines 41 – 57**).

7.12. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Keenan and the art of Mitchell with the art of Lewis to produce the claimed invention.

8. Dependent claims 5 and 7 - 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; "The Transmogrifier-2: A 1 Million Gate Rapid-Prototyping System", June 1998, IEEE Transactions on Very Large Scale Integration Systems), and Keenan (U.S. Patent Number 4,903,199), and Mitchell (U.S. Patent Number 6,230,119), in view of common knowledge in the art.

8.1. Dependent claims 5 and 7 – 12 are dependent on claim 4, and thereby inherit all of the rejected limitations of claim 4.

8.2. Regarding claim 8, Lewis appears to teach pre-loading at least one operation into the programmable logic device (**page 189, right-side column, item 8) Programming Time; page 196, left-side column, section G. Status, Power Monitoring, Host Communicaton, and Boot, first paragraph**).

8.3. Regarding claim 11, Lewis appears to teach returning test results to a user (**page 194, section C. Debugging Facilities**).

8.3.1. Regarding (**page 194, section C. Debugging Facilities**); it would have been obvious to return test results to a user.

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- 8.4.** Regarding claim 5, Lewis does not specifically teach that testing is performed in isolation of operations other than the at least one operation of a processor.
- 8.5.** Regarding claim 7, Lewis does not specifically teach adjusting the clock speed and repeatedly testing the operation in combination with a circuit.
- 8.6.** Regarding claim 9, Lewis does not specifically teach determining whether an operation is loaded into a programmable logic device and when the operation is loaded into the programmable logic device, omitting the downloading step.
- 8.7.** Regarding claim 10, Lewis does not specifically teach forwarding test data to the programmable logic device.
- 8.8.** Regarding claim 12, Lewis does not specifically teach that the method steps of claim 4 are implemented as computer readable code within a computer-readable signal-bearing medium.
- 8.9.** Regarding claim 5, Official Notice is taken that testing a single operation independent of other operations of a processor was old and well known in the art.
- 8.10.** Regarding claim 5, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to test a single operation independent of other operations of a processor in order to isolate a fault that occurs in the single operation, especially an intermittent fault.
- 8.11.** Regarding claim 7, Official Notice is taken that adjusting a clock speed and repeatedly testing an operation in combination with a circuit was old and well known in the art.

- 8.12.** Regarding claim 7, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to adjust a clock speed and repeatedly test an operation in combination with a circuit because this test would provide a threshold of clock speed when circuit failure occurred, especially intermittent failure.
- 8.13.** Regarding claim 9, Official Notice is taken that determining whether an operation is loaded into a programmable logic device and when the operation is loaded into the programmable logic device, omitting the downloading step was old and well known in the art.
- 8.14.** Regarding claim 9, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to determine whether an operation is loaded into a programmable logic device and when the operation is loaded into the programmable logic device, omitting the downloading step, because this test would eliminate a time consuming operation of downloading and its associated complexities.
- 8.15.** Regarding claim 10, Official Notice is taken that forwarding test data to a programmable logic device was old and well known in the art.
- 8.16.** Regarding claim 10, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to forward test data to a programmable logic device because test data is needed to test the function and speed of a processor operation.
- 8.17.** Regarding claim 12, Official Notice is taken that implementing method steps as computer readable code within a computer-readable signal-bearing medium was old and well known in the art.
- 8.18.** Regarding claim 12, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to implement method steps as computer readable code

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within a computer-readable signal-bearing medium because automating a manual method provides a timesavings and improved accuracy.

8.19. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to produce the claimed inventions.

9. Dependent claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; "The Transmogriker-2: A 1 Million Gate Rapid-Prototyping System", June 1998, IEEE Transactions on Very Large Scale Integration Systems), and Keenan (U.S. Patent Number 4,903,199), and Mitchell (U.S. Patent Number 6,230,119), in view of Wray (Wray, William C.; Greenfield, Joseph D; "Using microprocessors and microcomputers: the Motorola family", 1994), further in view of common knowledge in the art.

9.1. Dependent claim 6 is dependent on claim 4, and thereby inherits all of the rejected limitations of claim 4.

9.2. The art of Lewis is directed toward a rapid-prototyping system to emulate computer hardware systems (**page 188, Abstract, and section I. Introduction**).

9.3. The art of Wray is directed to using microprocessors (**Title**).

9.4. Lewis does not specifically teach that the processor operation for testing is one of read/write byte, read/write word, read/write double word, read/write quad word, burst read, burst write, dynamic memory access, protocol stack, interrupt process, and protected mode.

9.5. Wray appears to teach the operation of read/write byte (**page 646, column "Source Form(s)", row LDAA; and page 647, column "Source Form(s)", row STAA**).

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9.6. Official Notice is taken that testing the processor operations of read/write word, read/write double word, read/write quad word, burst read, burst write, dynamic memory access, protocol stack, interrupt process, and protected mode were old and well known in the art. The motivation to use these elements with the art of Lewis would have been obvious since these elements are commonly used computer operations, states or processes which would need to be tested during development of a processor.

9.7. The art of Wray and the art of Lewis are analogous art because they both contain the problem of testing a processor (**Lewis, page 194, section C. Debugging Facilities**) and (**Wray, page 346, Chapter 11 title "System Debugging"**).

9.8. The motivation to use the art of Wray with the art of Lewis would have been obvious because of the benefit recited in Wray to select the best methods to perfect a system under development (**page 346, section 11-1, item number 4**).

9.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to produce the claimed invention.

10. Independent claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; "The Transmogripher-2: A 1 Million Gate Rapid-Prototyping System", June 1998, IEEE Transactions on Very Large Scale Integration Systems), in view of Keenan (U.S. Patent Number 4,903,199).

10.1. The art of Lewis is directed toward a rapid-prototyping system to emulate computer hardware systems (**page 188, Abstract, and section I. Introduction**).

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10.2. The art of Keenan is directed to test systems for integrated circuits (column 1, lines 6 - 12).

10.3. Lewis appears to teach:

10.3.1. A computer readable signal-bearing medium on which is recorded computer readable program code (page 196, section G Status, Power Monitoring, Host Communication, and Boot).

10.3.1.1. Regarding (page 196, section G Status, Power Monitoring, Host Communication, and Boot); the section recites a host SUN Sparcstation, which typically would have memory and a disc drive, both of which would typically be a computer readable signal-bearing medium on which is recorded computer readable program code.

10.3.2. Downloading one or more processor operations into a programmable logic device (page 189, right-side column, item 8) Programming Time; page 196, left-side column, section G. Status, Power Monitoring, Host Communicaton, and Boot, first paragraph; page 188, section I. Introduction).

10.3.2.1. Regarding (page 189, right-side column, item 8) Programming Time; page 196, left-side column, section G. Status, Power Monitoring, Host Communicaton, and Boot, first paragraph; page 188, section I. Introduction); it would have been obvious that one or more processor operations are downloaded.

10.3.3. Selecting one or more of the processor operations (page 188, section Introduction).

10.3.3.1. Regarding (page 188, section Introduction); it would have been obvious that a system that emulates a processor will have one or more processor operations selected.

10.3.4. Selecting a clock speed at which to operate the programmable logic device (page 195, section F. Clocking; page 196, left-side column, section G. Status, Power Monitoring, Host Communication, and Boot, first paragraph).

10.3.4.1. Regarding (page 195, section F. Clocking; page 196, left-side column, section G. Status, Power Monitoring, Host Communication, and Boot, first paragraph); it would have been obvious that a clock speed is selected in order to program the clock speed.

10.3.5. Programming the programmable logic device to operate at the clock speed (page 195, section F. Clocking; page 196, left-side column, section G. Status, Power Monitoring, Host Communication, and Boot, first paragraph).

10.4. Lewis does not specifically teach repeatedly executing the selected one of the one or more processor operations.

10.5. Keenan appears to teach repeatedly executing the selected one of the one or more processor operations (column 1, lines 47 – 57; column 2, lines 25 – 30; and column 6, lines 24 – 30).

10.5.1. Regarding (column 1, lines 47 – 57; column 2, lines 25 – 30; and column 6, lines 24 – 30); it would have been obvious to repeatedly execute the selected one of the one or more processor operations.

- 10.6.** The art of Keenan and the art of Lewis are analogous art because they both contain the problem of testing integrated circuits (**Lewis, page 194, section C. Debugging Facilities**) and (**Keenan, column 1, lines 6 – 12**).
- 10.7.** The motivation to use the art of Keenan with the art of Lewis would have been obvious because of the benefit recited in Keenan that the method increases the speed of test program execution (**column 1, lines 1 – 12**).
- 10.8.** Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Keenan with the art of Lewis to produce the claimed invention.
- 11.** Dependent claims 14 – 15, and 17 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; “The Transmogripher-2: A 1 Million Gate Rapid-Prototyping System”, June 1998, IEEE Transactions on Very Large Scale Integration Systems) and Keenan (U.S. Patent Number 4,903,199), in view of common knowledge in the art.
- 11.1.** Dependent claims 14 – 15, and 17 - 20 are dependent on claim 13, and thereby inherit all of the rejected limitations of claim 13.
- 11.2.** Regarding claim 18, Lewis appears to teach pre-loading at least one operation into a programmable logic device (**page 189, right-side column, item 8) Programming Time; page 196, left-side column, section G. Status, Power Monitoring, Host Communicaton, and Boot, first paragraph**).
- 11.3.** Regarding claim 20, Lewis appears to teach returning test results to a user (**page 194, section C. Debugging Facilities**).

- 11.3.1.** Regarding (page 194, section C. Debugging Facilities); it would have been obvious to return test results to a user.
- 11.4.** Regarding claim 14, Lewis does not specifically teach determining whether a selected one of one or more processor operations is downloaded into the programmable logic device.
- 11.5.** Regarding claim 14, Lewis does not specifically teach downloading the selected one of the one or more processor operations into the programmable logic device when the selected one of the one or more processor operations is not downloaded into the programmable logic device.
- 11.6.** Regarding claim 15, Lewis does not specifically teach repeatedly executing the selected one of the one or more processor operations executing in isolation of operations other than the selected one of the one or more processor operations.
- 11.7.** Regarding claim 17, Lewis does not specifically teach adjusting the clock speed and repeatedly testing the operation in combination with a circuit.
- 11.8.** Regarding claim 19, Lewis does not specifically teach forwarding test data to the programmable logic device.
- 11.9.** Regarding claim 14, Official Notice is taken that determining whether a selected one of one or more processor operations is downloaded into the programmable logic device was old and well known in the art.
- 11.10.** Regarding claim 14, Official Notice is taken that downloading the selected one of the one or more processor operations into the programmable logic device when the selected one of the one or more processor operations is not downloaded into the programmable logic device was old and well known in the art.

11.11. Regarding claim 14, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to determine whether a selected one of one or more processor operations is downloaded into the programmable logic device because this test would eliminate a time consuming operation of downloading and its associated complexities.

11.12. Regarding claim 14, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to download the selected one of the one or more processor operations into the programmable logic device when the selected one of the one or more processor operations is not downloaded into the programmable logic device because it would only have been possible to test the selected operation when it is loaded into the programmable logic device.

11.13. Regarding claim 15, Official Notice is taken that repeatedly executing a processor operation in isolation of operations other than the selected one was old and well known in the art.

11.14. Regarding claim 15, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to repeatedly execute the selected one of the one or more processor operations, executing in isolation of operations other than the selected one of the one or more processor operations, because it would allow isolation of a fault that occurred in the single operation, especially an intermittent fault.

11.15. Regarding claim 17, Official Notice is taken that adjusting the clock speed and repeatedly testing an operation in combination with a circuit was old and well known in the art.

11.16. Regarding claim 17, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to adjust the clock speed and repeatedly test the

operation in combination with a circuit because this test would provide a threshold of clock speed when circuit failure occurs, especially intermittent failure.

11.17. Regarding claim 19, Official Notice is taken that forwarding test data to a programmable logic device was old and well known in the art.

11.18. Regarding claim 19, it would have been obvious to an artisan of ordinary skill at the time of Applicant's invention to forward test data to the programmable logic device because test data is needed to test the function and speed of a processor operation.

11.19. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to produce the claimed inventions.

12. Dependent claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (Lewis, David M.; Galloway, David R.; van Ierssel, Marcus; Rose, Jonathan; Chow, Paul; "The Transmogriifier-2: A 1 Million Gate Rapid-Prototyping System", June 1998, IEEE Transactions on Very Large Scale Integration Systems) and Keenan (U.S. Patent Number 4,903,199), in view of Wray (Wray, William C.; Greenfield, Joseph D; "Using microprocessors and microcomputers: the Motorola family", 1994), further in view of common knowledge in the art.

12.1. Dependent claim 16 is dependent on claim 13, and thereby inherits all of the rejected limitations of claim 13.

12.2. The art of Lewis is directed toward a rapid-prototyping system to emulate computer hardware systems (**page 188, Abstract, and section I. Introduction**).

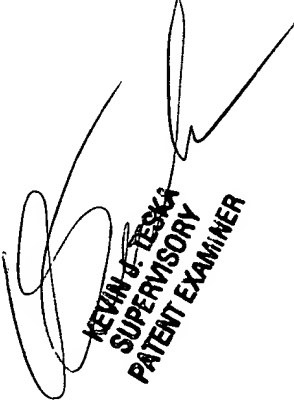
12.3. The art of Wray is directed to using microprocessors (**Title**).

- 12.4.** Lewis does not specifically teach that the selected one of the one or more processor operations for testing is one of read/write byte, read/write word, read/write double word, read/write quad word, burst read, burst write, dynamic memory access, protocol stack, interrupt process, and protected mode.
- 12.5.** Wray appears to teach the operation of read/write byte (page 646, column "Source Form(s)", row LDAA; and page 647, column "Source Form(s)", row STAA).
- 12.6.** Official Notice is taken that testing the processor operations of read/write word, read/write double word, read/write quad word, burst read, burst write, dynamic memory access, protocol stack, interrupt process, and protected mode were old and well known in the art. The motivation to use these elements with the art of Lewis would have been obvious since these elements are commonly used computer operations, states or processes which would need to be tested during development of a processor.
- 12.7.** The art of Wray and the art of Lewis are analogous art because they both contain the problem of testing a processor (Lewis, page 194, section C. Debugging Facilities) and (Wray, page 346, Chapter 11 title "System Debugging").
- 12.8.** The motivation to use the art of Wray with the art of Lewis would have been obvious because of the benefit recited in Wray to select the best methods to perfect a system under development (page 346, section 11-1, item number 4).
- 12.9.** Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to produce the claimed invention.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM – 5:30 PM.
14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RG


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